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09/536,452	03/28/2000	Ronny Ronen	02207/8754	5160

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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	8

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

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Office Action Summary	Application No. 09/536,452	Applicant(s) RONEN ET AL.
	Examiner David J. Huisman	Art Unit 2183

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☒ Claim(s) *18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 March 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-23 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: #7. Amendment 'A' as received on 4/14/2003.

Amendment Format Comments

3. The examiner has noted that amended claim 3 includes an added portion ("an address format control flag") that has not been underlined. In addition, amended claim 3 includes a deleted portion ("based at least in part on") that was not in the original claim 3.

Drawings

4. The drawings are objected to because of the following minor informalities: Please label component 140 in Fig.1 as a 64-bit address register for further clarity. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claim 18 objected to because of the following informalities: In line 2, please insert the word --that-- after the word "instruction". Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Killian et al., U.S. Patent No. 5,420,992 (herein referred to as Killian).

8. Referring to claim 1, Killian has taught a processor comprising:

a) means for executing an instruction of an application of a first bit size ported to a second bit size environment, the second bit size being greater than the first bit size. See column 2, lines 7-33.

b) means for confining the application to a first bit size address space subset (see column 19, lines 36-40), said means for confining comprising:

(i) means for truncating generated address references of the second bit size to the first bit size. See column 10, line 62, to column 11, line 5. In this passage, Killian has explained that the 32-bit architecture ignores overflow (i.e. performs truncation) during addition operations. Since Killian's system is backward compatible with the aforementioned 32-bit architecture, it follows that Killian's system would perform the same operations as the 32-bit architecture. Therefore, in overflow situations, truncation would be performed on 64-bit data (since the data path and register size of Killian's system is 64-bits) in order to obtain 32-bit data.

(ii) means for extending to the second bit size the truncated generated address references based at least in part on a setting of a predetermined control signal. See column 12, lines 45-65, and column 17, lines 27-31. Note that 32-bit data is sign extended for use in the extended architecture. Also, note that if the particular status register bits (predetermined control signal) specifies 32-bit mode, the addresses are sign-extended from 32 bits to 64 bits. In 64-bit mode, no sign extension occurs.

9. Referring to claim 2, Killian has taught a processor as described in claim 1. Killian has further taught that the first bit size is 32-bit and the second bit size is 64-bit. See column 3, lines 30-31, and column 5, lines 8-19.

10. Referring to claim 3, Killian has taught a processor as described in claim 1. Killian has further taught that the predetermined control signal includes an address format control flag. See column 17, lines 27-31. The particular status register bit(s) that control the size of the addresses, by specifying 32 or 64-bit mode, can be interpreted as an address format control flag.

11. Referring to claim 4, Killian has taught a processor as described in claim 3. Killian has further taught that the means for confining includes means for generating an address fault. See column 11, lines 3-5. The 32-bit address (which would be represented as an extended 64-bit number in the 64-bit environment) that is used to select a memory location in the address space subset is checked for a certain value and if that value exists, then an address error exception will occur.

12. Referring to claim 5, Killian has taught a processor as described in claim 1. Killian has further taught that the means for extending includes means for determining that the first bit size

address space subset is signed address space. See column 19, lines 36-40. From this passage it can be seen that the address space is from -2^{31} to $(2^{31}-1)$ which is also known as –2GB to +2GB.

13. Referring to claim 6, Killian has taught a processor as described in claim 1. Killian has further taught that the means for extending includes means for determining that the first bit size address space subset is unsigned address space. See column 13, lines 10-27, and Table 3A. Killian has disclosed Load-Byte-Unsigned (LBU) and Load-Halfword-Unsigned (LHU) instructions, which are zero-extended as opposed to sign extended. As an example, LBU will retrieve an 8-bit value from memory/cache, and zero-extend it to 64-bits, regardless of the most significant bit position. If this unsigned data were then used as an address to access memory, which is possible since Killian has also disclosed indirect jumps in Table 5B (where the contents of a specified register are used as an address to access memory), it would follow that the address space would be unsigned.

14. Referring to claim 7, Killian has taught a processor comprising:

a) a memory to store an instruction of an application ported from a first bit size environment to a second bit size environment, the second bit size being greater than the first bit size. See Fig.1 and column 7, lines 49-54. Note the existence of main memory and an instruction cache.

b) an instruction execution core coupled to said memory, said instruction execution core to execute the instruction of the application. See Fig.1. Note that data and instructions are retrieved from memory/cache by the EIC (component 25) and propagated along bus 30 to the execution unit.

c) said instruction execution core to determine that the application is confined to a first bit size address space subset. See column 19, lines 36-40.

d) said instruction execution core to generate an address reference of the second bit size as part of execution of the instruction. See column 12, lines 26-65.

e) said instruction execution core to truncate the generated address reference from the second bit size to the first bit size. See column 10, line 62, to column 11, line 5. In this passage, Killian has explained that the 32-bit architecture ignores overflow (i.e. performs truncation) during addition operations. Since Killian's system is backward compatible with the aforementioned 32-bit architecture, it follows that Killian's system would perform the same operations as the 32-bit architecture. Therefore, in overflow situations, truncation would be performed on 64-bit data (since the data path and register size of Killian's system is 64-bits) in order to obtain 32-bit data.

f) said instruction execution core to extend the truncated, generated address reference from the first bit size to the second bit size based at least in part on a setting of a predetermined control signal. See column 12, lines 45-65, and column 17, lines 27-31. Note that 32-bit data is sign extended for use in the extended architecture. Also, note that if the particular status register bits (predetermined control signal) specifies 32-bit mode, the addresses are sign-extended from 32 bits to 64 bits. In 64-bit mode, no sign extension occurs.

15. Referring to claim 8, Killian has taught a processor as described in claim 7. Killian has further taught that the application ported from a first bit size environment to a second bit size environment is an application ported from a 32-bit environment to a 64-bit environment. See column 3, lines 30-31, and column 5, lines 8-19.

16. Referring to claim 9, Killian has taught a processor as described in claim 7. Killian has further taught that the instruction execution core is to determine that the application is confined to a first bit size address space subset based at least in part on an address space control flag. See

column 17, lines 25-27. Note from columns 17-19, that based on the different modes, different address space subsets are used.

17. Referring to claim 10, Killian has taught a processor as described in claim 7. Killian has further taught that the instruction execution core is to extend the truncated, generated address reference from the first bit size to the second bit size based at least in part on an address format control flag. See column 17, lines 27-31. Note that if the "address format control flag" specifies 32-bit mode, the addresses are sign-extended from 32 bits to 64 bits. In 64-bit mode, no sign extension occurs.

18. Referring to claim 11, Killian has taught a processor as described in claim 7. Killian has further taught that the instruction execution core is to generate an address fault flag based at least in part on a comparison of the generated address reference and the extended, truncated, generated address reference. Recall from previous rejections that a generated 32-bit number is extended to a 64-bit number in Killian's system. From column 17, line 61, to column 18, line 7, Killian has disclosed that bit 31 of the 64-bit number is checked. If that value is 0, then an address fault has not occurred. However, if that value is 1, then an address exception has occurred. Bit 31, in a sense, represents an overflow bit in that when that bit is set, then the 32-bit application has crossed the 32-bit address space boundary and a fault has occurred. It should be noted that a comparison would inherently be performed to check bit 31. And, this comparison is related to both the original 32-bit address and the extended 64-bit version.

19. Referring to claim 12, Killian has taught a processor as described in claim 11. Killian has further taught that the instruction execution core is to generate an address fault flag based at least in part on an address fault control flag. See Fig.5E. In the upper-right corner of the figure,

different types of address faults (R3ERR, R2ERR, R1ERR, and R0ERR) are coupled to a multiplexer which is controlled by an address fault control flag VA(63..62). This value is used to help generate an address fault flag (output line denoted as ADDRESS ERROR), if one exists for the corresponding mode.

20. Referring to claim 13, Killian has taught a processor as described in claim 7. Killian has further taught that the memory is a cache memory. See column 7, lines 50-52.

21. Referring to claim 14, Killian has taught a processor as described in claim 7. Killian has further taught that the processor is a 64-bit processor. See column 2, lines 16-41, and column 3, lines 30-31. Killian has disclosed that the registers and data path, along with memory addresses, are 64 bits wide. Therefore, Killian has taught a 64-bit processor.

22. Referring to claim 15, Killian has taught a method to confine an application to an address space subset, the method comprising the steps performed by the processor of claim 7. Therefore, claim 15 is rejected for the same reasons set forth in the rejection of claim 7.

23. Referring to claim 16, Killian has taught a method as described in claim 15. Furthermore, claim 16 is rejected for the same reasons set forth in the rejection of claims 7 and 8.

24. Referring to claim 17, Killian has taught a method as described in claim 16. Furthermore, claim 17 is rejected for the same reasons set forth in the rejection of claim 8.

25. Referring to claim 18, Killian has taught a method as described in claim 15. Furthermore, claim 18 is rejected for the same reasons set forth in the rejection of claim 9.

26. Referring to claim 19, Killian has taught a method as described in claim 15. Furthermore, claim 19 is rejected for the same reasons set forth in the rejection of claim 10.

27. Referring to claim 20, Killian has taught a method as described in claim 15. Killian has further taught that extending the truncated, generated address reference from the first bit size to the second bit size includes sign-extending the truncated, generated address reference from the first bit size to the second bit size based at least in part on an address format control flag. See column 17, lines 27-31. Note that if the "address format control flag" specifies 32-bit mode, the addresses are sign-extended from 32 bits to 64 bits. In 64-bit mode, no sign extension occurs.

28. Referring to claim 21, Killian has taught a method as described in claim 15. Killian has further taught that extending the truncated, generated address reference from the first bit size to the second bit size includes zero-extending the truncated, generated address reference from the first bit size to the second bit size based at least in part on an address format control flag. Recall from the rejection of claim 6 that the LBU and LHU instructions involve unsigned data (which can be used as an address) that is zero-extended as opposed to sign extended. Furthermore, the processor will know to zero-extend such unsigned data when it encounters the appropriate opcode. The opcode's unique value will tell the system to use zero-extended, unsigned data. Therefore, the opcode is considered to be an address format control flag.

29. Referring to claim 22, Killian has taught a method as described in claim 15. Furthermore, the processor of claim 11 performs the method of claim 22. Therefore, claim 22 is rejected for the same reasons set forth in the rejection of claim 11.

30. Referring to claim 23, Killian has taught a method as described in claim 22. Furthermore, the processor of claim 12 performs the method of claim 23. Therefore, claim 23 is rejected for the same reasons set forth in the rejection of claim 12.

Response to Arguments

31. Applicant's arguments filed on April 14, 2003 have been fully considered but they are not persuasive.

32. Applicant has argued the novelty of amended claim 1 in substance that:

> "...extending to the second bit size the truncated generated address references based at least in part on a setting of a predetermined control signal is not disclosed or suggested by Killian et al.. Specifically, the portion of Killian et al. (see column 17, lines 27-31) asserted by the examiner as anticipating the predetermined control signal is incorrect. Rather, the asserted portion is more accurately analogized to the address space control flag, since it defines whether addresses are treated as 32-bit of 64-bit addresses. The predetermined control signal recited in claim 1 is used to define whether the truncated, 32-bit addresses are either zero extended or sign extended. There is no equivalent structure in Killian et al. that is used to explicitly specify whether the truncated 32-bit addresses are either zero extended or sign extended."

This argument is not found persuasive for the following reasons:

a) Since the Applicant has not specifically defined, within the claim, how the "predetermined control signal" is used for purposes of extending, the predetermined control signal is merely a signal that plays a part in the extension of the truncated generated address references to a second bit size based on its set value (as defined by claim 1). The control bit in the status register taught by Killian et al. in column 17, lines 27-31, meets this definition in that if the control bit(s) specify that the machine is in 32-bit mode, it is also specifying that 32-bit addresses will be sign-extended to 64 bits. While the Applicant may be correct in arguing that the "address format control flag" taught by Killian et al. is more accurately analogized to the address space control flag, the "address format control flag" of Killian et al. still results in 32-bit references being extended to 64-bits. Although Applicant's address format control flag determines whether to

zero-extend or sign-extend a 32-bit value, the absence of this limitation in claim 1 allows for anticipation by Killian et al.. This reasoning also applies to amended claims 7 and 15.

Conclusion

33. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (703) 305-7811. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

DJH
David J. Huisman
May 16, 2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
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